REMARKS

It is believed that the above amendments and following remarks attend to each and every rejection and objection presented in the pending September 14, 2005 office action. Claims 1-21 remain pending, with claims 1, 9, 16, 19, 20 and 21 being independent. Claims 1, 9, 16, 19, 20 and 21 are amended.

Specification

Paragraph [0001] is amended to insert information of related applications, as requested in paragraph 2 of the pending office action. Reconsideration is requested.

Claim Objections

Claims 1, 9, 16, 19, 20 and 21 are objected to because of formalities. Claims 1, 9, 16, 19, 20 and 21 are amended, as requested in paragraph 3 of the pending office action, to replace acronym HLSN with 'highest level signal name (HLSN)'. No new matter is added.

Claim Rejections – 35 U.S.C. §102

Claims 1-4 and 19-21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Publication No. US 2003/0237067 A1 to Mielke et al. (hereinafter "Mielke"). Respectfully, we disagree.

As way of background, the following summary may help clarify the differences between the immediate application and Mielke. The immediate application teaches, for example, a method and system for determining wire capacitance for a VLSI circuit design. A wire capacitance database is generated based upon indicia of the most accurate one of a plurality of wire capacitance data sources for each net in at least a plurality of blocks of the VLSI circuit design. Cumulative wire capacitance is then determined for each highest level signal name (HLSN) in each of the blocks in a portion of the VLSI circuit design to be analyzed.

On the other hand, Mielke discloses a system and method for automating a static-timing analysis of an integrated circuit design. Mielke is concerned with automating the process of analyzing an integrated circuit design and not about circuit analysis. For example, Mielke does not identify a most accurate wire capacitance

from more than one wire capacitance data sources. In Mielke, FIGs. 2 and 5, only one 'parasitics file' is shown; and Mielke makes no disclosure that identifies a most accurate wire capacitance value from more than one source. The concerns of Mielke are clearly different from those of the immediate application.

To anticipate a claim, Mielke must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." MPEP 2131 citing Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Mielke does not teach every element of claims 1-4 and 19-21.

Amended claim 1 recites a method for determining wire capacitance for a VLSI circuit design, including the steps of:

a) determining hierarchical blocks of a portion of the design;

b) storing, for a plurality of the blocks, indicia of a most accurate one of a plurality of wire capacitance data sources;

c) generating a wire capacitance database with an entry for each net, in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

d) generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram; and

e) using the hierarchical connectivity model and said wire capacitance database to determine a cumulative wire capacitance value for each highest level signal name (HLSN) in each of the blocks in a portion of the design to be analyzed.

On the other hand, in Mielke, FIG. 5, a single source of parasitic information (e.g., parasitic file 256) is shown. Mielke does not show a plurality of wire capacitance data sources, as required by step b) of claim 1. Paragraph [0014] of the immediate specification teaches that wire capacitance values may be generated from

an analysis of a design block by a wire capacitance source 110(*) such as a design analyzer and/or a CAD tool estimator. Clearly, more than one source for wire capacitance values is required to allow indication of a most accurate one. Paragraph [0014] of the immediate specification further describes a data source indicator 103 that indicates the source of the wire capacitance data (e.g., wire capacitance values acquired through an E-CAD tool functioning as a capacitance estimator source), as required by step b). Step c) requires that a wire capacitance database be generated using information stored in at least one of the wire capacitance data sources.

Mielke also does not disclose generating a database of wire capacitance information as required by step c). Step d) requires that a hierarchical connectivity model be generated using a single type of connectivity data for each of the blocks using either a layout or schematic diagram. Mielke does not disclose using either a schematic or layout diagram to build a model. Mielke does not disclose – anywhere – determining a cumulative wire capacitance value for a highest level signal name (HLSN) in each of the blocks in a portion of the design to be analyzed, as required by step e). For at least these reasons, Mielke cannot anticipate claim 1.

Reconsideration of claim 1 is requested.

Claims 2-4 depend from claim 1 and benefit from like argument. However, these claims have additional features that patentably distinguish over Mielke. For example, claim 2 recites that the cumulative wire capacitance value for each HLSN is determined by summing the wire capacitance for each net of each HLSN. Mielke does not disclose summing the wire capacitance value for each net of each HLSN. The Examiner asserts that steps 704-708 of FIG. 7 teach how cumulative wire capacitance for each HLSN can be determined. Respectfully, Mielke recites only that "the computing device 104 uses the top-level circuit representation to generate the top-level parasitics as indicated in step 706 ... next, in step 708, the computing device 104 is programmed to reduce the parasitics in accordance with the particular timing model type selected for the functional block of interest." See Mielke paragraphs 80 and 81. Respectfully, the Examiner is requested to clarify how this teaches the features of claim 2, as we contend that the Mielke disclosure does not anticipate claim 2.

Claim 3 recites that a single type of connectivity data is selected from the layout if all of the connectivity data for the portion of the design to be analyzed is available from the layout. Claim 4 recites wherein the hierarchical connectivity model for the design is generated by using layout connectivity, if that layout is available for a given block; otherwise, if no layout is available for the given block, then by using schematic connectivity data. Mielke make no suggestion of using schematic connectivity data for generating a hierarchical connectivity model. For at least these reasons, Mielke cannot anticipate claims 3-4.

Reconsideration of claims 2-4 is requested.

Amended claim 19 recites a system for determining wire capacitance for a VLSI circuit design, including:

a) means for determining all hierarchical blocks of a portion of the design;

b) means for storing, for a plurality of the blocks, indicia of the best available one of a plurality of wire capacitance data sources;

c) means for generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

d) means for generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram; and

e) means for calculating a cumulative wire capacitance value for each high level signal name (HLSN) in each of the blocks in a portion of the design to be analyzed, using the hierarchical connectivity model and said wire capacitance database.

Mielke does not disclose a means for storing indicia of the best available one of a plurality of wire capacitance data sources, as required by step b) of claim 19. Mielke does not disclose means for generating a wire capacitance database as required by step c). Mielke further does not disclose means for generating a hierarchical

connectivity model for the design using a single type of connectivity data for each of the blocks, as required by step d). And, Mielke does not disclose means for determining a cumulative wire capacitance value for a HLSN in each of the blocks in a portion of the design to be analyzed, as required by step e). For at least these reasons, Mielke cannot anticipate claim 19.

Reconsideration of claim 19 is respectfully requested.

Amended claim 20 recites a software product with instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for determining wire capacitance for a VLSI circuit design, including:

a) instructions for determining all hierarchical blocks of a portion of the design;

b) instructions for storing, for a plurality of the blocks, indicia of the best available one of a plurality of wire capacitance data sources;

c) instructions for generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

d) instructions for generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram; and

e) instructions for using the hierarchical connectivity model and said wire capacitance database to determine a cumulative wire capacitance value for each high level signal name in each of the blocks in a portion of the design to be analyzed.

Mielke does not disclose storing indicia of the best available one of a plurality of wire capacitance data sources, as required by element b) of claim 20. Mielke does not disclose generating a database of wire capacitance information using information stored in at least one of the wire capacitance data sources, as required by element c). Mielke does not disclose using a single type of connectivity data to generate a

hierarchical connectivity model, wherein the single type of connectivity data is either a schematic or layout diagram, as required by element d). And, Mielke does not determining a cumulative wire capacitance value for a highest level signal name (HLSN) in each of the blocks in a portion of the design to be analyzed, as required by element e). For at least these reasons, Mielke cannot anticipate claim 20.

Reconsideration of claim 20 is requested.

Amended claim 21 recites a system for determining wire capacitance for a VLSI circuit design, including:

a) means for determining all hierarchical blocks of a portion of the design;

b) means for storing, for a plurality of the blocks, indicia of the most accurate one of a plurality of wire capacitance data sources;

c) means for generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources; and

d) means for generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either layout or a schematic diagram;

e) wherein the hierarchical connectivity model and said wire capacitance database is used to determine a cumulative wire capacitance value for each high level signal name in each of the blocks in a portion of the design to be analyzed.

Mielke does not disclose storing indicia of the most accurate one of a plurality of wire capacitance data sources, as required by element b) of claim 21. Mielke does not disclose generating a database of wire capacitance information using information stored in at least one of the wire capacitance data sources, as required by element c). Mielke does not disclose using a single type of connectivity data to generate a hierarchical connectivity model, wherein the single type of connectivity data is either a schematic or layout diagram, as required by element d). Mielke does not disclose

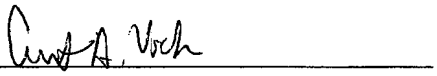
determining a cumulative wire capacitance value for a HLSN in each of the blocks in a portion of the design to be analyzed, as required by element e). For at least these reasons, Mielke cannot anticipate claim 21.

Reconsideration of claim 21 is respectfully requested.

We appreciate the Examiner's indication of allowable subject matter of claims 5-18. In view of the above amendments and arguments, we now respectfully request reconsideration of claims 1-4 and 19-21.

It is believed that no fees are due in connection with this amendment. If any additional fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

By: 

Curtis A. Vock, Reg. No. 38,356
LATHROP & GAGE L.C.
4845 Pearl East Circle, Suite 302
Boulder, CO 80301
Telephone: (720) 931-3011
Facsimile: (720) 931-3001